# Lab 2 Structural Report

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing “yes” at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? Yes

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here: Jiwon Youn

Student Name: Wonhee Lee  
Student ID: 54872959  
Date Completed: 05-03-2020  
Time Spent: Reviewing Digital Design Material: 1h   
 Design/Preparation Work: 15h  
 VHDL Coding & Debugging: 8h

## Structural Overview

90%

Outputs satisfy the condition. It works with the testbench. However, not sure with the minimum clock cycle. The equations were too long so it was hard to type it correctly in the code. The first FSM design I came up with was not satisfying, which output came out quite late than expected. So, I fixed the truth table and started again. There are total 4 cases tested in testbench. One 10$ and two 5$, which was initially provided, one 20$, one 10$ and one 20$, and 3 5$ and cancelled and one 20$. Over 20$, 20$, and cancelled are tested.

## Lab 2 Truth Table(s)

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| State | CurrState3 | CurrState2 | CurrState1 | CurrState0 | Input | Permit | ReturnChange | NextState3 | NextState2 | NextState1 | NextState0 | NextState |
| Initial | 0 | 0 | 0 | 0 | 000 | 0 | 0 | 0 | 0 | 0 | 0 | Initial |
| Initial | 0 | 0 | 0 | 0 | 001 | 0 | 0 | 0 | 0 | 0 | 1 | Five\_T |
| Initial | 0 | 0 | 0 | 0 | 010 | 0 | 0 | 0 | 0 | 1 | 0 | Ten\_T |
| Initial | 0 | 0 | 0 | 0 | 100 | 0 | 0 | 0 | 1 | 1 | 1 | Twenty |
| Initial | 0 | 0 | 0 | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 1 | Cancel |
| Five\_T | 0 | 0 | 0 | 1 | 000 | 0 | 0 | 0 | 1 | 0 | 0 | Five\_W |
| Five\_T | 0 | 0 | 0 | 1 | 001 | 0 | 0 | 0 | 0 | 0 | 1 | Five\_T |
| Five\_T | 0 | 0 | 0 | 1 | 010 | 0 | 0 | 0 | 0 | 0 | 1 | Five\_T |
| Five\_T | 0 | 0 | 0 | 1 | 100 | 0 | 0 | 0 | 0 | 0 | 1 | Five\_T |
| Five\_T | 0 | 0 | 0 | 1 | 111 | 0 | 0 | 0 | 0 | 0 | 1 | Five\_T |
| Ten\_T | 0 | 0 | 1 | 0 | 000 | 0 | 0 | 0 | 1 | 0 | 1 | Ten\_W |
| Ten\_T | 0 | 0 | 1 | 0 | 001 | 0 | 0 | 0 | 0 | 1 | 0 | Ten\_T |
| Ten\_T | 0 | 0 | 1 | 0 | 010 | 0 | 0 | 0 | 0 | 1 | 0 | Ten\_T |
| Ten\_T | 0 | 0 | 1 | 0 | 100 | 0 | 0 | 0 | 0 | 1 | 0 | Ten\_T |
| Ten\_T | 0 | 0 | 1 | 0 | 111 | 0 | 0 | 0 | 0 | 1 | 0 | Ten\_T |
| Fifteen\_T | 0 | 0 | 1 | 1 | 000 | 0 | 0 | 0 | 1 | 1 | 0 | Fifteen\_W |
| Fifteen\_T | 0 | 0 | 1 | 1 | 001 | 0 | 0 | 0 | 0 | 1 | 1 | Fifteen\_T |
| Fifteen\_T | 0 | 0 | 1 | 1 | 010 | 0 | 0 | 0 | 0 | 1 | 1 | Fifteen\_T |
| Fifteen\_T | 0 | 0 | 1 | 1 | 100 | 0 | 0 | 0 | 0 | 1 | 1 | Fifteen\_T |
| Fifteen\_T | 0 | 0 | 1 | 1 | 111 | 0 | 0 | 0 | 0 | 1 | 1 | Fifteen\_T |
| Five\_W | 0 | 1 | 0 | 0 | 000 | 0 | 0 | 0 | 1 | 0 | 0 | Five\_W |
| Five\_W | 0 | 1 | 0 | 0 | 001 | 0 | 0 | 0 | 0 | 1 | 0 | Ten\_T |
| Five\_W | 0 | 1 | 0 | 0 | 010 | 0 | 0 | 0 | 0 | 1 | 1 | Fifteen\_T |
| Five\_W | 0 | 1 | 0 | 0 | 100 | 0 | 0 | 1 | 0 | 0 | 0 | Over |
| Five\_W | 0 | 1 | 0 | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 1 | Cancel |
| Ten\_W | 0 | 1 | 0 | 1 | 000 | 0 | 0 | 0 | 1 | 0 | 1 | Ten\_W |
| Ten\_W | 0 | 1 | 0 | 1 | 001 | 0 | 0 | 0 | 0 | 1 | 1 | Fifteen\_T |
| Ten\_W | 0 | 1 | 0 | 1 | 010 | 0 | 0 | 0 | 1 | 1 | 1 | Twenty |
| Ten\_W | 0 | 1 | 0 | 1 | 100 | 0 | 0 | 1 | 0 | 0 | 0 | Over |
| Ten\_W | 0 | 1 | 0 | 1 | 111 | 0 | 0 | 1 | 0 | 0 | 1 | Cancel |
| Fifteen\_W | 0 | 1 | 1 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 1 | Fifteen\_T |
| Fifteen\_W | 0 | 1 | 1 | 0 | 001 | 0 | 0 | 0 | 1 | 1 | 1 | Twenty |
| Fifteen\_W | 0 | 1 | 1 | 0 | 010 | 0 | 0 | 1 | 0 | 0 | 0 | Over |
| Fifteen\_W | 0 | 1 | 1 | 0 | 100 | 0 | 0 | 1 | 0 | 0 | 0 | Over |
| Fifteen\_W | 0 | 1 | 1 | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 1 | Cancel |
| Twenty | 0 | 1 | 1 | 1 | 000 | 1 | 0 | 0 | 0 | 0 | 0 | Initial |
| Twenty | 0 | 1 | 1 | 1 | 001 | 1 | 0 | 0 | 0 | 0 | 0 | Initial |
| Twenty | 0 | 1 | 1 | 1 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | Initial |
| Twenty | 0 | 1 | 1 | 1 | 100 | 1 | 0 | 0 | 0 | 0 | 0 | Initial |
| Twenty | 0 | 1 | 1 | 1 | 111 | 1 | 0 | 0 | 0 | 0 | 0 | Initial |
| Over | 1 | 0 | 0 | 0 | 000 | 1 | 1 | 0 | 0 | 0 | 0 | Initial |
| Over | 1 | 0 | 0 | 0 | 001 | 1 | 1 | 0 | 0 | 0 | 0 | Initial |
| Over | 1 | 0 | 0 | 0 | 010 | 1 | 1 | 0 | 0 | 0 | 0 | Initial |
| Over | 1 | 0 | 0 | 0 | 100 | 1 | 1 | 0 | 0 | 0 | 0 | Initial |
| Over | 1 | 0 | 0 | 0 | 111 | 1 | 1 | 0 | 0 | 0 | 0 | Initial |
| Cancel | 1 | 0 | 0 | 1 | 000 | 0 | 1 | 0 | 0 | 0 | 0 | Initial |
| Cancel | 1 | 0 | 0 | 1 | 001 | 0 | 1 | 0 | 0 | 0 | 0 | Initial |
| Cancel | 1 | 0 | 0 | 1 | 010 | 0 | 1 | 0 | 0 | 0 | 0 | Initial |
| Cancel | 1 | 0 | 0 | 1 | 100 | 0 | 1 | 0 | 0 | 0 | 0 | Initial |
| Cancel | 1 | 0 | 0 | 1 | 111 | 0 | 1 | 0 | 0 | 0 | 0 | Initial |

Permit ReturnChange

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| C1C0  C3C2 | 00 | 01 | 11 | 10 |  | C1C0  C3C2 | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 0 | 0 |  | 00 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 1 | 0 |  | 01 | 0 | 0 | 0 | 0 |
| 11 | 0 | 0 | 0 | 0 |  | 11 | 0 | 0 | 0 | 0 |
| 10 | 1 | 0 | 0 | 0 |  | 10 | 1 | 1 | 0 | 0 |

## Lab 2 Final Equations

**Permit** = C3C2’C1’C0’ + C3’C2C1C0

**ReturnChange** = C3C2’C1’

**NextState3 =** C3’C2C1C0’I2’I1I0’ + C3’C2C1’I2I1I0 + C3’C2C1’I2I1’I0’ + C3’C2C0’I2I1I0 + C3’C2C0’I2I1’I0’ + C3’C1’C0’I2I1I0

**NextState2 =** C3’C2C1C0’I2’I1’I0 + C3’C2C1’C0I2’I0’ + C3’C2C1’I2’I1’I0’ + C3’C2’C1I2’I1’I0’ + C3’C2’C1’C0’I2I1’I0’ + C3’C2’C0I2’I1’I0’

**NextState1 =** C3’C2C1C0’I2’I1’ + C3’C2C1’I2’I1I0’ + C3’C2C1’I2’I1’I0 + C3’C2’C1C0I1’I0’ + C3’C2’C1I2I1I0 + C3’C2’C1I2’I1I0’ + C3’C2’C1I2’I1’I0 + C3’C2’C0’I2I1’I0’ + C3’C2’C0’I2’I1I0’

**NextState0 =** C3’C2C1C0’I2’I1’ + C3’C2C1’C0I2’I1’ + C3’C2C1’I2’I1I0’ + C3’C2C0’I2I1I0 + C3’C2’C1’I2I1’I0’ + C3’C2’C1’I2’I1’I0 + C3’C2’C0I2I1I0 + C3’C2’C0I2I1’I0’ + C3’C2’C0I2’I1I0’ + C3’C2’C0I2’I1’I0 + C3’C1C0’I2’I1’I0’ + C3’C1’I2I1I0

Used K-map for Permit and ReturnChange

Used Quine–McCluskey Minimization Technique for NextStates

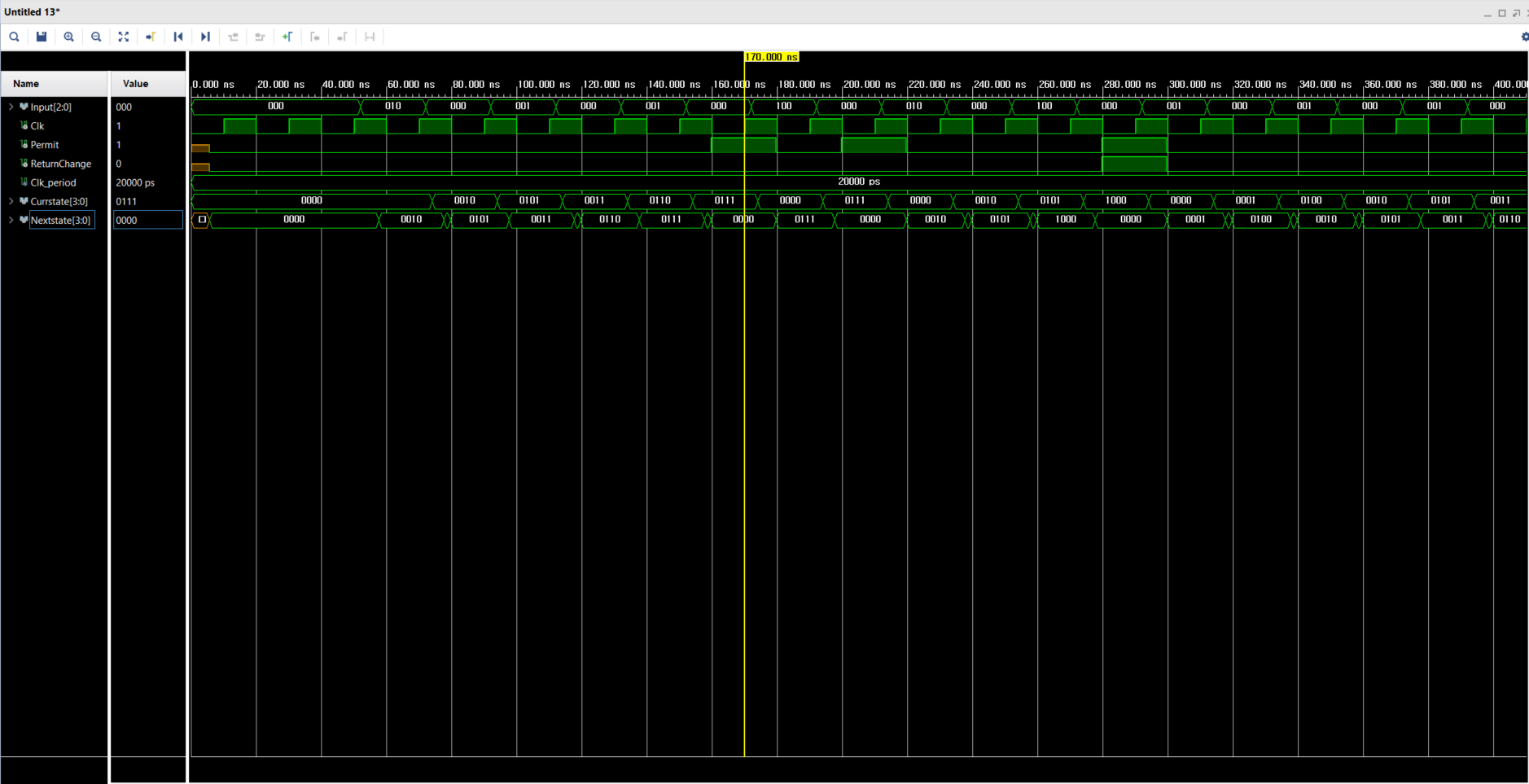
## Lab 2 Minimum Clock Cycle

Minimum clock cycle: 15.4 ns

Explain how you derived your minimum clock cycle (as discussed in EECS 31) here.

Drew the circuit, calculated the delay, and chose the longest path. Among all the outputs and NextState variable, the longest delay is the delay for the entire circuit.

## Lab 2 Structural Simulation Graph



## Lab 2 Structural and Behavioral Simulation Graph Comparisons

Fixed the problem with the clock cycle.